

Action = Pattern Data * Timing Data (Limited by TimeSet) * Waveset * Drive

FIG._1

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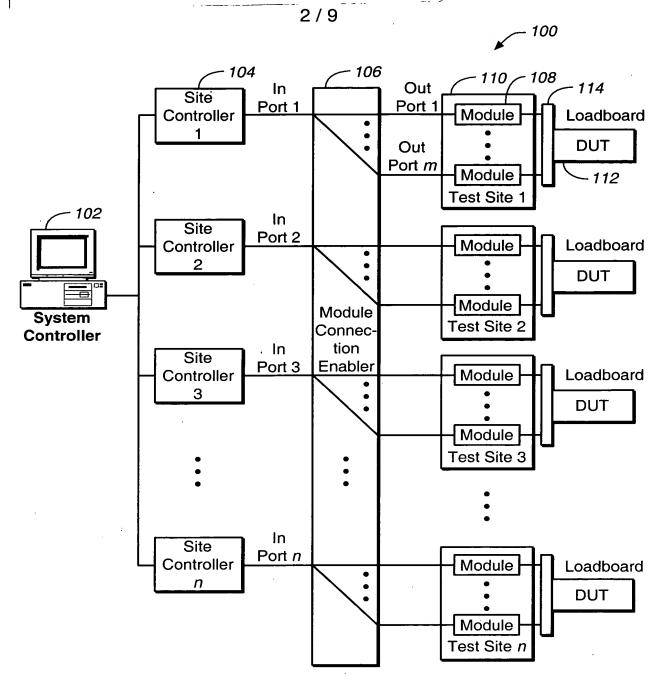


FIG._2

Filed: February 6, 2004 Docket No.: 333772000800 Sheet 3 of 9 3/9 <u>200</u> 226 225 224 System Controller **Tools** Framework Classes - 220 Tools 222 Standard Interfaces SYSC ← SITEC Communications Library - 230 243 - 242 **User Test Plan** User Test Classes - 246 Standard 244 Test Classes Framework Classes Controller - 240 Standard Interfaces 245-Module-Level Interfaces Site 247 248 Module Commands Implementation - 249 250-**Backplane Communications Library** PCI Backplane Driver 261 280-Backplane Emulation HW Backplane - 262 282-Framework Backplane Module Emulation in SW Chassis Slot IF <u> 283</u> - 263 Simulation IF - 264 Module Emulation <u>284</u> Module Hardware Loadboard Loadboard Modules Simulation - 260 Simulation IF Hardware IF Loadboard 286 Hardware Loadboard Simulation - *265* **DUT Simulation IF** Verilog PLI C/C++289 DUT 287-- *266* **DUT Verilog** DUT C/C++ 288-Model Model 281 293 291 FIG._3 Interface Module Development 290 296 User External 292 298 **SYSTEM** 294 Key

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TPL Compiler

Source
Code
404

DLLs
406

FIG._4

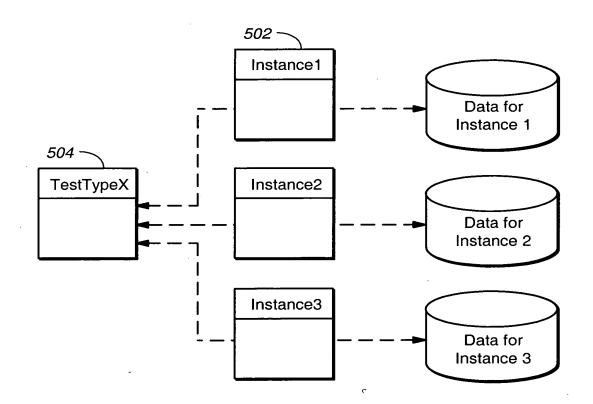
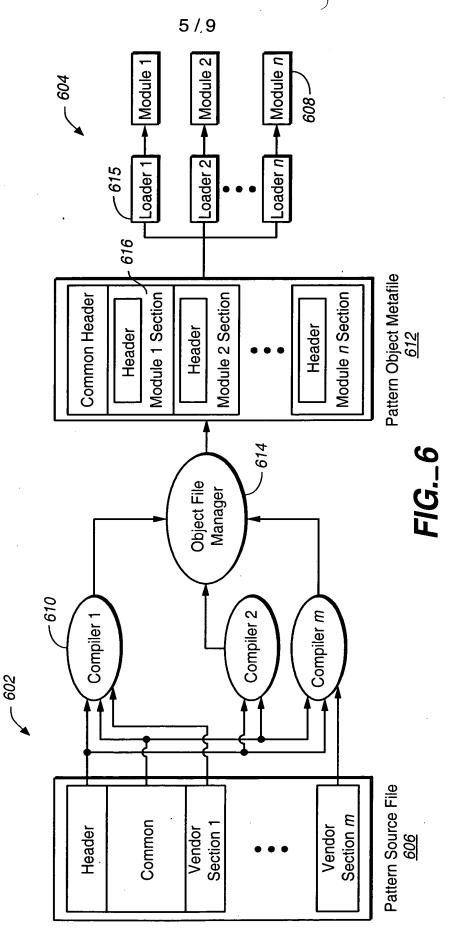


FIG._5

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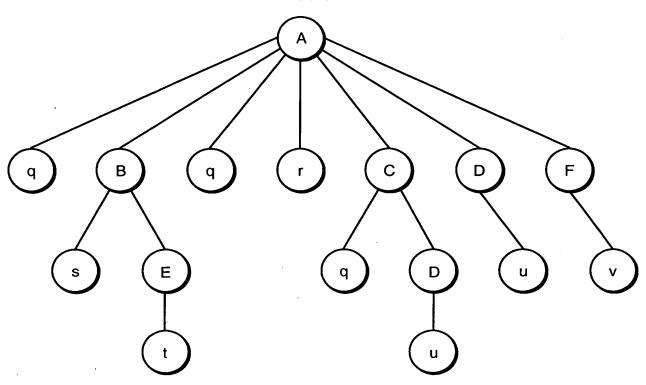


FIG._7

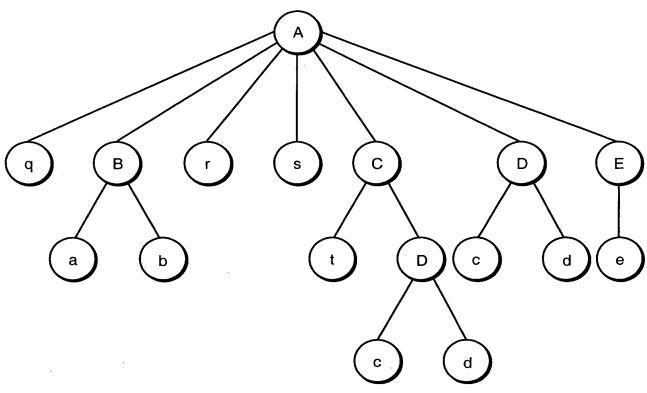


FIG._8

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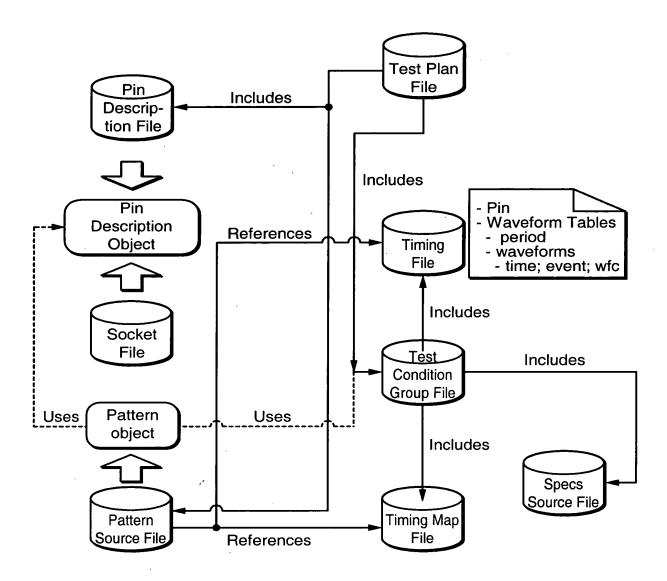
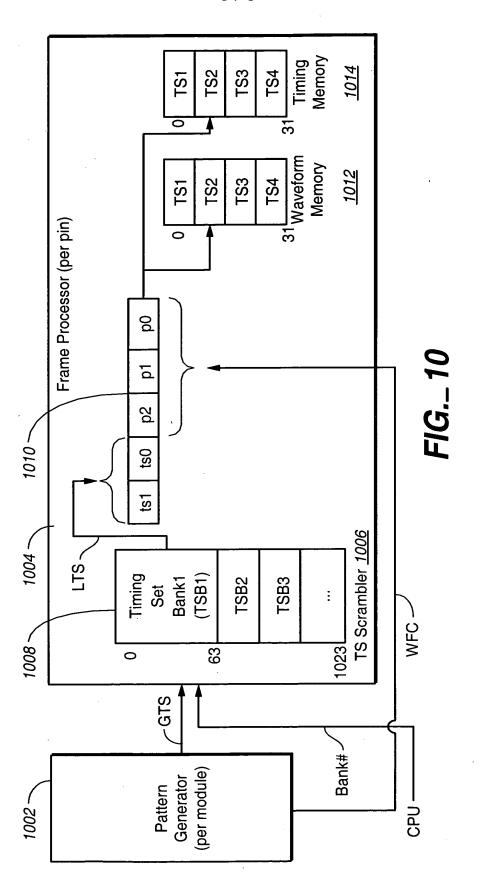


FIG._9

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